WHAT IS CLAIMED IS:

1. A logical simulation system comprising:

delay information operating part which receives a dispersion rule file in which information on dispersion in a chip having electrical and physical characteristics which influence the operation of an integrated circuit to be analyzed is described and which receives design information of the integrated circuit to prepare a delay information file in consideration of each influence of said information on said dispersion on the basis of said dispersion rule file and said design information; and

logical simulation part which receives said design information and said delay information file to carry out a logical simulation of the integrated circuit.

2. A logical simulation system as set forth in claim 1, wherein said delay information operating part corrects said design information on the basis of said dispersion, and

said delay information file includes the corrected design information.

3. A logical simulation system as set fourth in claim 1, which further comprises an information classifying unit which classifies said information on said dispersion into groups of an optional size, said groups constituting said chip, and

wherein said delay information file is prepared so that the influence of said dispersion is considered for every said group.

4. A logical simulation system as set forth in claim 1, wherein said design information includes actual configuration information which is information on the position of a cell of the integrated circuit in an actual configuration, and

said logical simulation system further comprises a file editing unit which receives said dispersion rule file to cause said information on said dispersion to correspond to said actual configuration information to edit said dispersion rule file.

5. A logical simulation system as set forth in claim 1, wherein said electrical and physical characteristics include a power supply voltage, and

said logical simulation includes verification whether abnormality is caused in the transmission of said signal by the difference in said power supply voltage in the same chip.

6. A logical simulation system as set forth in claim 2, wherein said electrical and physical characteristics include a power supply voltage, and

said delay information operating unit calculates dispersion of signal level caused by dispersion in said power supply voltage, and a delay time of signal transmission caused by the dispersion of the signal level.

7. A logical simulation system as set forth in claim 1, wherein said design information includes information on wiring,

said delay information operating unit divides said information on wiring into segments corresponding to said size of said group, and

said delay information file is prepared so that the influence of said dispersion is considered for every said segment.

8. A logical simulation method comprising:

preparing a dispersion rule file in which information on dispersion in a chip having electrical and physical characteristics which influence the operation of an integrated circuit being to be analyzed is described;

preparing a delay information file in consideration of each influence of said dispersion on the basis of said dispersion rule file and said design information; and

executing a logical simulation of the integrated circuit using said design information and said delay information file.

9. A logical simulation method as set forth in claim 8, which

further comprises correcting said design information on the basis of said dispersion, and

wherein said delay information file includes the corrected design information.

10. A logical simulation method as set fourth in claim 8, which further comprises classifying said information on said dispersion into groups of an optional size, said groups constituting said chip, and

wherein said delay information file is prepared so that the influence of said dispersion is considered for every said group.

11. A logical simulation method as set forth in claim 8, wherein said design information includes actual configuration information on the position of a cell of the integrated circuit in an actual configuration, and

said logical simulation method further comprises causing said information on said dispersion to correspond to said actual configuration information to edit said dispersion rule file.

12. A logical simulation method as set forth in claim 8, wherein said electrical and physical characteristics include a power supply voltage, and

said executing of said logical simulation includes verifying whether abnormality is caused in the transmission of said signal by the difference in said power supply voltage in the same chip.

13. A logical simulation method as set forth in claim 8, wherein said electrical and physical characteristics include a power supply voltage, and

said executing of said logical simulation further comprises calculating dispersion of signal level caused by dispersion in said power supply voltage, and a delay time of signal transmission caused by the dispersion of signal level.

14. A logical simulation method as set forth in claim 10, wherein said design information includes information on wiring,

said logical simulation method further comprises dividing said information on wiring into segments corresponding to said size of said group, and

said delay information file is prepared so that the influence of said dispersion is considered for every said segment.

15. A computer-readable recorded medium for use in a computer which receives design information of an integrated circuit to be analyzed to execute a logical simulation of the integrated circuit, said medium having recorded a program for causing said computer to execute a logical simulation method, said method 8comprising:

preparing a dispersion rule file in which information on dispersion in a chip having electrical and physical characteristics which influence the operation of the integrated circuit is described;

preparing a delay information file in consideration of each influence of said dispersion on the basis of said dispersion rule file and said design information; and

executing a logical simulation of the integrated circuit using said design information and said delay information file.

16. A computer readable recorded medium according to claim 15, wherein said logical simulation method further comprises correcting said design information on the basis of said dispersion, and

said delay information file includes the corrected design information.

17. A computer readable recorded medium according to claim 15, wherein said logical simulation method further comprises classifying said information on said dispersion into groups of an optional size, said groups constituting said chip, and

said delay information file is prepared so that the

influence of said dispersion is considered for every said group.

18. A computer readable recorded medium according to claim 15, wherein said design information includes actual configuration information on the position of a cell of the integrated circuit in an actual configuration, and

said logical simulation method further comprises causing said information on said dispersion to correspond to said actual configuration information to edit said dispersion rule file.

19. A computer readable recorded medium according to claim 15, wherein said electrical and physical characteristics include a power supply voltage, and

said executing of said logical simulation includes verifying whether abnormality is caused in the transmission of said signal by the difference in said power supply voltage in the same chip.

20. A computer readable recorded medium according to claim 16, wherein said electrical and physical characteristics include a power supply voltage, and

said executing of said logical simulation further comprises calculating dispersion of signal level caused by dispersion in said power supply voltage, and a delay time of signal transmission caused by the dispersion of signal level.

21. A computer readable recorded medium according to claim 15, wherein said design information includes information on wiring,

said logical simulation method further comprises dividing said information on wiring into segments corresponding to said size of said group, and

said delay information file is prepared so that the influence of said dispersion is considered for every said segment.